Implementation of Low Power Clocking System Using Sequential Elements

D.Aneel Kumar 1*, N.Satyanarayana 2*

1. II.M.Tech (VLSI), Dept of ECE, AM Reddy Memorial College of Engineering & Technology, Petlurivaripalem.
2. Asst.Prof, Dept. of ECE, AM Reddy Memorial College of Engineering & Technology, Petlurivaripalem.

Abstract: *The design of low power digital systems this paper proposes sequential elements are low power flip-flops play a vital role for power consumption. The existing digital systems are using Flip flops and latches are consumes more power due to redundant clocking and transitions systems. Mainly the power dissipation in digital system by any clock distribution of sequential circuit in any chip almost 30% to 60% of the total power dissipation by the circuit. In integrated circuits design clock is the most important signal present in the chip, those clock signal s are synchronizing signals which provides timing reference for computation of any work in digital systems. This paper proposes a power of sequential circuits are reduces the overall chip power.*

Index Terms: clocking system, Low power, Flip-flop.

1. INTRODUCTION

The last two decades the VLSI designers are concerns the reliability, performance, area, and cost. At present power consideration was also gave secondary importance. However this has begun to change increasingly power are being comparable weights of area and speed considerations. At present now a days the one of the important factor is that excessive power consumption is becoming the limiting factor to integrate more transistors on a single chip in different modules. Unless the power dramatically reduced the resulting heat will limit the feasible packing and performance of VLSI design circuits. At present the digital systems designs are synchronous which implies both Flip-flops and latches plays a main role and then control paths. Challenges of this paper are low power consumption methodologies for synchronous systems of the flip-flops and latches. Based these methodologies to save in these flip-flops and latches without compromising the performance. For power consumption measurement several factors including frequency, supply voltage, capacitance, and short circuit current.

P= Pdynamic + Pshort circuit + Pleakage (1)

The above equation, Pdynamic is called the switching power p= αCv2f. P short circuit is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short period

Pshort circuit = Ishort circuit * Vdd.

Pleakage is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the sub threshold leakage current.

Pleakage current = Ileakage current * Vdd.

**** D.Aneel Kumar***
II.M.Tech (VLSI), Dept of ECE, AM Reddy Memorial College of Engineering & Technology,

Based on the above factors, there are various techniques for lowering the power consumption shown as follows: In Double Edge Triggering, Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. Double clock edge triggering method reduces the power by decreasing frequency. Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock Distribution, the flip-flop should be a low swing flip- flop. The low swing method reduces the power consumption by decreasing voltage.

There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional capture flip-flop (CCFF)) or clock gating, conditional discharge flip-flop (CDFF). In Conditional Operation, there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to avoid the redundant switching. In Clock Gating, when a certain block is idle, we can disable the clock signal to that block to save power. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

In Reducing Short Current Power, split path can reduce the short current power, since p- MOS and n-MOS are driven by separate signals. In Reducing Capacity of Clock Load, 80% of non clocked nodes have switching activity less than 0.1.

This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity.

II. METHODOLOGY OF LOW POWER CLOCKING SYSTEM

Flip-Flops are the basic elements for storing data and they are the fundamental building blocks for all sequential circuits. Flip-flops their content change only either at the rising or at falling edge of the enable signal. After the rising or falling edge of the enable signal the flip-flop's content remains constant even if the input data changes. However in the part of clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. CDFF and CCFF both have large clocked transistors. For example, CDFF used 15 clocked loads and CCFF used 14 clocked transistors. In respect to this, conditional data mapping flip-flop used only 7 clocked transistors, which resulting in about 50% reduction in the number of clocked transistors load, so due to this CDMFF used less power than CCFF and CDFF. This result illustrate that the by reducing clocked loads numbers help in achieving low power. Since CDMFF is better in performance than CCFF and CDFF in respect of power consumption.

CDMFF ha less number of clocked loads but it has redundant clocking in it and it has floating node as a drawback. To result in efficient and error free implementation of low power register element, a Clocked Pair Shared flip-flop (CPSFF) is proposed. In this circuit of clocked-pair-shared flip-flop, a clocked pair (N3, N4) is shared by first and second stage of the latching part as which is shown in figure 1 below

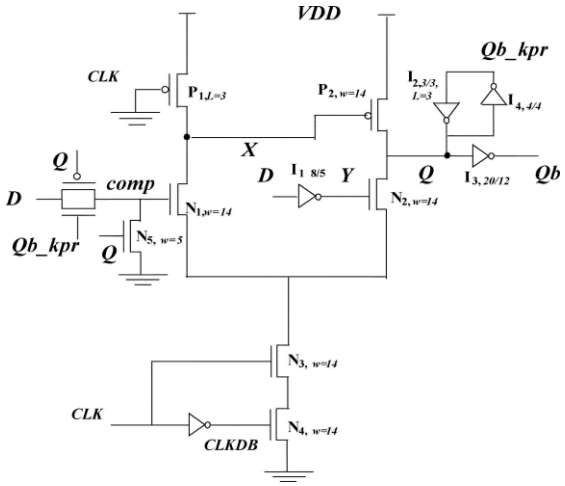

Fig.1. clocked pair shared Flip-flop.

The pseudo NMOS transistor that is PMOS, P1, is used to charge the internal node X despite being using the two clocked pre charging transistors (P1, P2) which is used in CDMFF. By comparing CDMFF with CPSFF, a total of three clocked loads are reduced in CPSFF, such that the clock load seen by the clock driver is minimized, resulting in an efficient design. CPSFF uses four clocked loads despite of seven clocked loads which is used in CDMFF, it result in about 40% reduction in number of clocked loads. Additional to this the internal node X is connected to supply voltage Vdd with the help of a pseudo NMOS P1, so is not floating point is now present, and result also shows an improvement in the noise robustness of node X. When input D stays at HIGH level then Q=1, here N5 is kept ON, N1 will be kept off to avoid the redundant transient activity at node X, as well as in any short circuit current. PMOS P2 is allowed to pull Q to high level when D switches to 1 value. Then second NMOS branch (N2) is in charge for pulling down the output of Q if D = LOW value and Y=1when the clock pulse is arrives. PMOS present in N1 should turn on NMOS N2 when D=LOW. Although P1 is always ON, short circuit only occurs one time when D makes a transition from LOW to HIGH, and then discharge path is disconnected after two gates delay. After all that, if at this time also D remains at HIGH, then the discharge path is already disconnected by N1; there would be no short circuit. Here the clocked-pseudo-NMOS scheme is different from the general idea of common pseudo-NMOS logic. In the previous one we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly scaled to guarantee a correct noise margin. CPSFF uses three less clocked loads, which by default leads to about 40% reduction in number of clocked loads. It achieves 25% less clock driving power consumption than CDMFF, which improves power efficiency.

III. PROPOSED LOW POWER CLOCKED PASS TRANSISTOR FLIP-FLOP DESIGN

This paper concentrate on pass transistor logical family of designing circuit is using only one clocking transistor do it will consume less power in the clock network of the flip flops when compared to all other designed circuits.

We have 6 transistors excluding the not gates also. When we use this design we will be having much reduced power and area when we compared to the other existing designs. At the same time due to reduce the number of transistors count then automatically we can reduce the overall switching delay, area, power consumption. The proposed circuit will be acting as a good sequential element when compared to other flip-flop design.
The graph represents the input & output characteristics of our proposed system from that we can clearly understand how it works as negative edge triggered flip-flop. There is some nano seconds delay is there even though it's a negligible amount only. Those delays can be further reduced by reducing the sizes of the transistor we are using in this circuit. Or by reducing the nano meter technology also we can reduce the constraints. The Layout design of the proposed new flip-flop is shown in the figure 3 the area of that is mentioned at the downside of the layout.

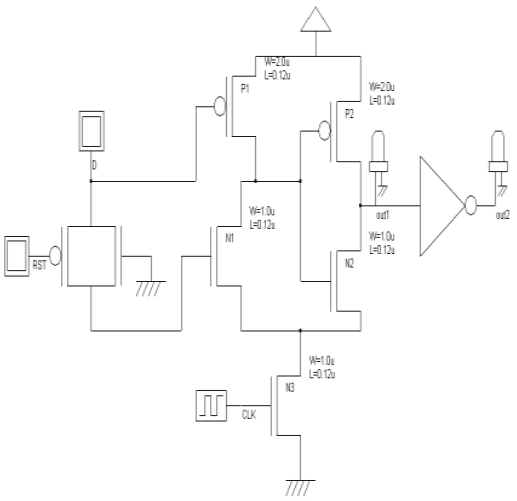

Fig.2.proposed low power clocked pass transistor flip-flop

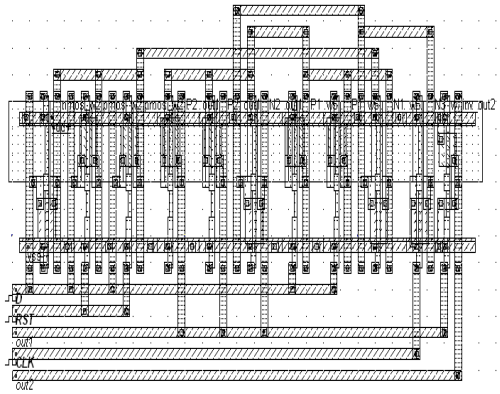

Fig.3. Layout of the LCPTFF proposed design

Thus the Our Proposed Low Power Clocked Pass Transistor flip-flop (LCPTFF Fig.2) design shows much less power & Area constraints than the Existing two Flip-Flop designs. As well as the Proposed design will be having very less clock delay when compared to all other circuits. So it can be used in all the future sequential elements for high speed low SOC'c manufacturing.

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IV. CONCLUSION

This proposed paper work is a variety of design techniques for low power clocking system are reviewed. This is the effective method to reducing the capacity of clock load by minimizing number of clocked transistors are elaborated. The following approach is a novel CPSFF is proposed it can reduce local clock transistor number by about 40%. And to view of power consumption of clock driver of the new cpsff outperforms prior arts in flip-flop design by about 25%.

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