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A NOVEL APPROACH ON POWER EFFICIENT ARITHMETIC APPLICATIONS BASED ON CMOS ADDERS

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ABSTRACT

This project presents a novel high speed and low power CMOS full adder cells are designed which is one of the basic blocks of latest electronic system design method. Now a day's energy efficiency is most required feature in digital electronic system for efficient performance of portal application which signifies the PDP, and also it measure the consumed energy for switching event. The proposed paper shows the complementary CMOS of logical style for the implementation of combinational circuit design of low voltage, low power, and small power delays are concern relatively less area.

I. INTRODUCTION

Technologically improvement of World VLSI design system application are specifically DSP architectures, microprocessors, FIR filter and systolic array design of fundamental requirement of operation such as adder. Thus Full adders are the core of many arithmetic operations such as addition subtraction, multiplication, division and address generation. In the majority of systems, the adder is part of the critical path that determines the overall performance of the system. As stated, the system's overall performance would affected by PDP exhibited by the full-adder. To enhance the performance of the full adder cell results of great interest. By considering this facts the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. In advancement of mobile product which worked with a high throughput capability makes the design of low-power adder module another significant goal to be achieved. Power dissipation can be cause by three major components in complementary metal oxide semiconductor (CMOS) circuit's namely switching power short circuit power and static power. Reducing any of these components will accounts for lower power consumption for the whole system design. In this paper, the report to design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor When compared with other ones reported previously low-power arithmetic modules.

II. RELATED WORK

A full adder could be a combinational circuit that forms the

arithmetic sum of three input bits. It consists of three inputs and two outputs. In our design, we have designated the three inputs as A, B and C. The third input C represents carry input to the first stage. The outputs are SUM and CARRY. Fig 1 shows the logic level diagram of full adder. The Boolean expressions for the SUM and CARRY bits are as shown below.

SUM=A⊕B⊕C

CARRY=A.B+A.CIN+B.C

SUM bit is the EX-OR function of all three inputs and CARRY bit is the AND function of thee inputs. The Table I of a full adder is shown. The truth table also indicates the status of the CARRY bit, that is to say, if that c array bit has been generated or deleted or propagated. Depending on the fig1. Logic diagram of full adder, depending on the status of input bits A and B, the CARRY bit either generated or detected.

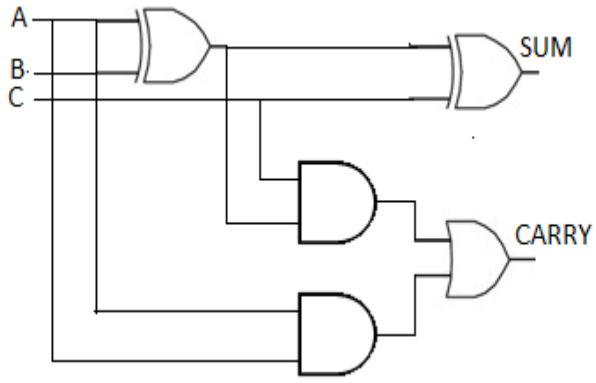

Fig.1. Logic diagram of a full adder.

Table I: truth table of a full adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

If either one of A or B inputs is '1', then the previous carry is just propagated, as the sum of A and B is '1'. If both A and B are '1's then carry is generated because summing A and B would make output SUM '0' and CARRY '1'. If both A and B are '0's then summing A and B would give us '0' and any previous carry is added to this SUM making CARRY bit '0'. This is in effect deleting the CARRY.

III. PROPOSED METHODOLOGY

After studying the truth table of full adder in Table 1, it can be observed that the So output is equal to the (A XOR B) value when C=0, and equal to (A XNOR B) when C=1. From this observation we conclude that a multiplexer will be used to obtain the respective value based upon the Carry input, as stated earlier. Using the same scenario, the Co output is equal to the (A AND B) value when C=0, and (A OR B) value when C=1. In the similar way, carry will be used to drive a multiplexer. Hence, an energy efficient logic scheme to design a full adder cell can be formed by a logic block to get the (AXOR B) and (AXOR B) signals, other block to obtain (A AND B) and (A OR B) signals, and two multiplexers being driven by the Carry input to generate the So and Co outputs, as shown in Figure 2.

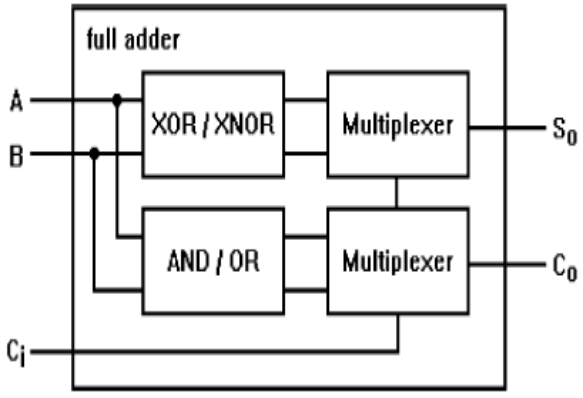

Fig.2. Alternative Logic scheme for energy efficient full adder.

The proposed method features and advantages that can be expected for this energy efficient logic structure are given below,

- No requirement of internal signal for controlling the select line of multiplexers. Instead of the Carry input signal, it which has full voltage swing and without delay is used to drive the select line of multiplexers, which reduces the overall propagation delay of full adder.
- To reduces the capacitive load for the carry input because it is connected only to some transistor gates and not to some drain or source terminals, where the diffusion capacitance is becoming very large. Hence, the overall delay for larger modules where the carry signal falls on the critical path can be reduced.
- The propagation delay can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates for the So and Co outputs; this criteria is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining).
- By interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, the placement of buffers at the full-adder outputs can be implemented which can improve the performance for load-sensitive applications.

Depending on the results obtained in two new full-adders will be been designed using the logic styles DPL and SR-CPL.

Fig. 2 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output. In Fig. 3 presents the SR-CPL logic Style which will be used to build XOR/XNOR gates. AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively in both cases and a pass-transistor based multiplexer to get the Co output.

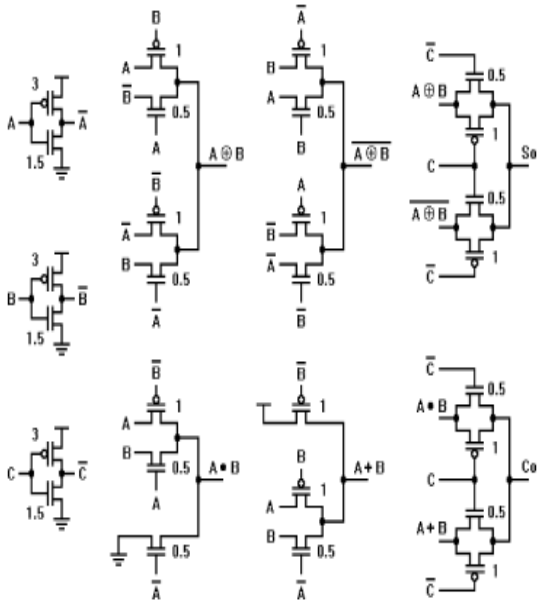

Fig.2. **Full-adder designed with the Energy Efficient structure using a DPL logic style.**

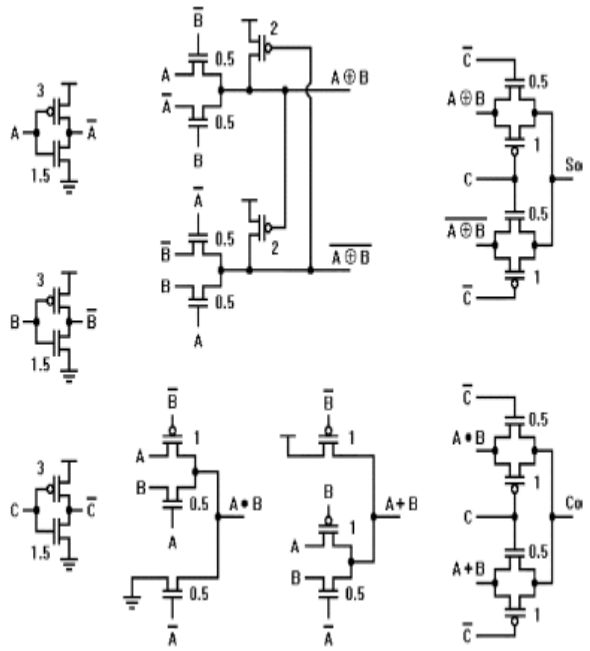

Fig.3. **Full-adder designed with the Energy Efficient structure using a SR-CPL logic style.**

IV. CONCLUSION

A novel design of high speed low power full adder cells based an alternative logic approach has been presented. Here we present a great improvement of power delay metric for the proposed adders, and compared to several existing realizations. Full adders designed using improved logical structure of DPL, and SR-CPL logic style, less delay of around 720ps and less power consumption of around 840 μW of an overall reduction of 30% respect to the best feature one of the other adders been compared to general about 50% to the other. Future we can do some work for designing of high speed low power full adders, to consider alternative logical structure constitute logic blocks (XOR/XNOR, AND, OR, and MUX cells).

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