REDUCED DC LINK VOLTAGE FOR LOAD COMPENSATION BY DSTATCOM USING NON-STIFF SOURCE

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Abstract: The distribution static compensator (DSTATCOM) is used for load compensation in power distribution network. In this paper, a new topology for DSTATCOM applications with non-stiff source is proposed. The proposed topology enables DSTATCOM to have a reduced dc-link voltage without compromising the compensation capability. It uses a series capacitor along with the interfacing inductor and a shunt filter capacitor. With the reduction in dc-link voltage, the average switching frequency of the insulated gate bipolar transistor switches of the DSTATCOM is also reduced. Consequently, the switching losses in the inverter are reduced. Detailed design aspects of the series and shunt capacitors are discussed in this paper. A simulation study of the proposed topology has been carried out using power systems computer-aided design simulator and the results are presented. Experimental studies are carried out to verify the proposed topology.

Keywords: dc-link voltage, DSTATCOM, hybrid topology, non-stiff source

1.   INTRODUCTION

The proliferation of power electronics devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network. To improve the quality of power, active power filters have been proposed. The distribution static compensator (DSTATCOM) is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the load is remote from the distribution substation and is associated with feeder impedance.

In the presence of feeder impedance, the inverter switching's distorted both the PCC voltage and the source currents. In this situation, the source is termed as non- stiff. If the same control algorithm for the stiff sources is used for the non- stiff sources, the reference currents generated will be erroneous; the load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives, however, better results. The state feedback control of the shunt filter capacitor eliminates the switching frequency components in the terminal voltages and source currents.

The compensation performance of any active filter depends on the voltage rating of dc-link capacitor. In general, the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. This is done in order to ensure a proper compensation at the peak of the source voltage. In the authors discuss the current distortion limit and loss of control limit, which states that the dc-link voltage should be greater than or equal to √6 times the phase voltage of the system for distortion-free compensation.

When the dc-link voltage is less than this limit, there is insufficient resultant voltage to drive the

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currents through the inductances so as to track the reference currents. Reference value of the dc-bus capacitor voltage mainly depends upon the requirement of reactive power compensation of the active power filter.

The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak of source voltage at the PCC. Due to these criteria, many researchers have used a higher value of dc capacitor voltage based on their applications.

2. CONVENTIONAL AND PROPOSED DSTATCOM

In this section, the conventional and proposed topologies of the DSTATCOM are discussed in detail. Fig. 1.1 shows the power circuit of the neutral clamped VSI topology-based DSTATCOM which is considered the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently and tracking is smooth with less number of switches when compared to other VSI topologies. In this figure, vsa, vsb, and vsc are source voltages of phases a, b, and c, respectively. Similarly, vta, vtb, and vtc are the terminal voltages at the PCC. The source currents in three phases are represented by isa, isb, and isc and load currents are represented by ila, ilb, and ilc.

The shunt active filter currents are denoted by if a, if b, if c, and io represents the current in the neutral leg. Ls and Rs represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance are represented by Lf and Rf, respectively. The load constituted of both linear and nonlinear loads are as shown in this figure. The dc-link capacitors and voltages across them are represented by Cdc1 = Cdc2 = Cdc and Vdc1 = Vdc2 = Vdc, respectively. The current through the dc link is represented by the idc. In this topology, the voltage across each dc-link capacitance is chosen

as 1.6 times the peak value of the source voltages as given.Fig. 2.5 shows the equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM. It is a combination of the conventional DSTATCOM topology with a capacitor Cf in series with the interfacing shunt branch of the active filter and a capacitor Csh in shunt with the active filter. This topology is referred to as hybrid topology. The passive capacitor Cf has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the conventional topology will reduce the dc-link requirement and reduces the average switching frequencies of the switches.
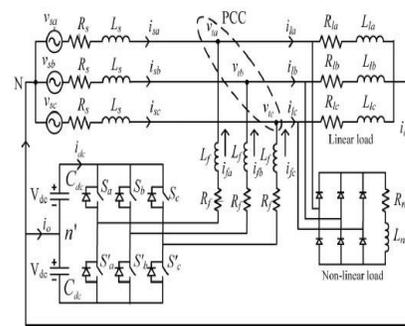
Equivalent circuit of neutral clamped VSI topology
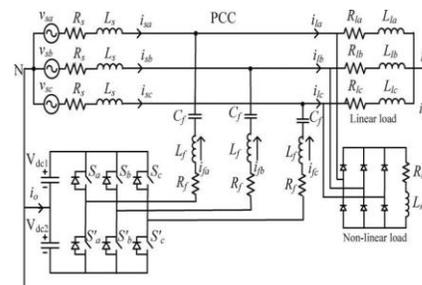
Equivalent circuit diagram of proposed neutral clamped VSI topology-based DSTATCOM

3. DESIGN OF VSI PARAMETERS

The parameters of the VSI need to be designed carefully for better tracking performance. The most important parameters that need to be

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taken into consideration while designing conventional VSI are dc-link voltage Vdc, dc storage capacitor Cdc, interfacing inductance Lf, and switching frequency fsw. A detailed design procedure of VSI parameters is given; based on the following equations; the parameters of the conventional VSI topology are chosen. The dc-link capacitor value is given by

$$C_{dc} = \frac{\left(2X - \frac{x}{z}\right)nT}{(1.8V_m)^2 - (1.4V_m)^2} \quad (1)$$

where Vm is the peak value of the source voltage, X is the kVA rating of the system, n is the number of cycles, and T is the time period of each cycle. The interfacing inductance is given by

$$L_f = \frac{1.6V_m}{4hf_{swmax}} \quad (2)$$

Where

$$h = \sqrt{\frac{k_1}{k_2} \frac{2(m^2 - 1)}{4m^2}} f_{swmax} \quad (3)$$

Where k1 and k2 are proportionality constants, fswmax is the maximum switching frequency of the switch, fswmin is minimum switching frequency of the switch, and m is given by

$$m = \frac{1}{\sqrt{1 - f_{swmin}/f_{swmax}}}.$$

As mentioned earlier, the dc-link voltage reference (Vdcref) of the conventional VSI topology has been taken as 1.6 Vm for each capacitor.

Each capacitor consider a three-phase system with 230-V line-to-neutral voltage. The hysteresis band h is taken as 0.5 A. The interfacing inductance Lf is computed to be 26 mH. The base kVA rating of the system is taken as 15 kVA. Cdc is computed and found to be 3300 μF. The system parameters are given in Table 3.1 for the conventional VSI topology.

TABLE 3.1. System Parameters

System Quantities	Values
System voltages	230V(line to neutral),50Hz
Linear load	$Z_{la}=34+j47.5\Omega$
	$Z_{lb}=81+j39.6\Omega$
Feeder impedance	$Z_s=1+j3.141\Omega$
Nonlinear load	Three phase full bridge rectifier load feeding a R-L load of 150Ω-
VSI parameters	$C_{dc}=3300\mu F$, $V_{dcref}=1.6V_m=520v$ $L_f=26mH$, $R_f=0.1\Omega$
PI Controller gains	$K_p=2$,$K_i=0.5$
Hysteresis band (h)	$\pm0.5A$

4. DESIGN OF SHUNT CAPACITOR FFOR THE PROPOSED VSI TOPOLOGY

A.   In the presence of the feeder impedance the terminal voltages are distorted due to unbalance and nonlinear load currents. Thus, these voltages can no longer be used to generate the reference quantities. In order ti improve the performance, positive –sequence voltages at the terminal are extracted using the power invariant instantaneous symmetrical transformation and are used for generating the reference currents. If the filter current resonant at a frequency then we get

$$C_{shr} = \frac{1}{\omega_r^2 L_s}.$$

Where Шr = fundamental frequency Ш0.

A straightforward insertion of shunt passive capacitor at the PCC may lead to stability issues and also with the increase in the capacitance value, the source current and terminal voltages increase. The use state feedback is one option to

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solve this problem.

B.   Design of series capacitor in the proposed VSI topology

The fundamental filter current drawn by the shunt filter capacitor is neglected while designing the capacitor value. This is because the impedance between the PCC and ground becomes very high when Csh is chosen much smaller than Csho at fundamental frequency. The design of the series capacitor depends upon the value to which the dc-link voltage is reduced. When the loads are nonlinear then the proposed hybrid topology is more efficient. Then the minimum impedance in the system is given as:

$$Z_{\min} = \frac{V_{\text{base}}^2}{S_{\max}} = |R_l + jX_l| \text{ (say)}.$$

In order to achieve the unity power factor, the shunt filter current needs to supply the required load reactive current. The filter current and load current in a particular phase are given as:

$$I_{\text{filter}} = \frac{V_{\text{inv1}} - V_{t1}}{R_f + j(X_{lf} - X_{cf})}$$

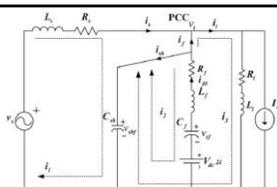$$I_{\text{load}} = \frac{V_{t1}}{R_l + jX_l}$$

Neglected the interfacing resistance and equating the imaginary parts of the above equation is given as:

$$\frac{V_{t1} X_l}{R_l^2 + X_l^2} = \frac{V_{\text{inv1}} - V_{t1}}{(X_{lf} - X_{cf})^2}(X_{lf} - X_{cf})$$

Where Xlf =2πfLf, Xl=2πfL1 etc...

C.   State Feedback Control

To derive the state space model of the system the single line diagram of the proposed DSTATCOM is considered.

single line diagram of the proposed DSTATCOM It contains three forcing functions:

1)   The source voltage
2)   Non-linear load current
3)   Switching variable

The control vector is given as: u=[uc]
The state space equation is given as:

$$\dot{x} = Ax + B_1 v_s + B_2 u + B_3 I_h$$

Where

$$A = \begin{bmatrix} -R_s/L_s & 0 & 0 & -1/L_s & 0 \\ 0 & -R_f/L_f & 0 & 1/L_f & -1/L_f \\ 0 & 0 & -R_l/L_l & 1/L_f & 0 \\ 1/C_{\text{sh}} & -1/C_{\text{sh}} & -1/C_{\text{sh}} & 0 & 0 \\ 0 & 1/C_f & 0 & 0 & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L_s \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ -V_{\text{dc}}/L_f \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad B_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ -1/C_f \\ 0 \end{bmatrix}.$$

The state variables can be written as:

$$i_s = i_1; \quad i_{sh} = i_1 - i_2 - i_3; \quad i_l = i_3;$$

$$i_f = i_3 - i_1; \quad v_{cf} = v_{cf}; \quad v_{shf} = v_t.$$

The transfoemed network of the z parameter is given as: Thus by using the above equation we get:

$$\min f = \sum_{i=1}^{N} [\text{Re}[\lambda_i(\Lambda_i - \Gamma_{1i}K)] - \xi_i(\Lambda_i - \Gamma_{1i}K)]$$

The feedback control ler is designed to ensure robustness under parametric variations. The control law is defined as:

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$$u_c = -K(z - z_{\text{ref}})$$

Where Zref = desired state vector

The optimization function is given as:

$$\min f = \sum_{i=1}^{N}[\text{Re}[\lambda_i(\Lambda_i - \Gamma_{1i}K)] - \xi_i(\Lambda_i - \Gamma_{1i}K)]$$

Subjected to

$$K_{\min 1} < K_1 < K_{\max 1}, \quad K_{\min 2} < K_2 < K_{\max 2}.$$

Here K=[K1 K2 0 0 0] and N is the number of possible operating conditions. The feedback gains are to be foundas K=[13.6759   6.5009   0 0 0].

D.   Generation of Reference Compensator Currents Unbalanced And Distored Voltages

In this paper the reference currents are generated using instantaneous symmetrical component theory and are given as:

$$i_{fa}^* = i_{la} - i_{sa}^* = i_{la} - \frac{v_{ta} + \gamma(v_{tb} - v_{tc})}{\Delta}(P_{\text{lavg}} + P_{\text{loss}})$$

$$i_{fb}^* = i_{lb} - i_{sb}^* = i_{lb} - \frac{v_{tb} + \gamma(v_{tc} - v_{ta})}{\Delta}(P_{\text{lavg}} + P_{\text{loss}})$$

$$i_{fc}^* = i_{lc} - i_{sc}^* = i_{la} - \frac{v_{tc} + \gamma(v_{ta} - v_{tb})}{\Delta}(P_{\text{lavg}} + P_{\text{loss}})$$

Where

$$\Delta = \sum_{j=a,b,c} v_{tj}^2, \gamma = \tan\varphi/\sqrt{3}.$$

Where Pavg =average load power

Ploss =switching and ohmic losses

In this paper, the load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at PCC unbalanced and distorted. If the loads are unbalanced and distorted it is not possible to get the balanced and sinusoidal currents after compensation.

The positive-sequence voltages that are extracted from the terminal voltages vta, vtb, and vtc are the reference filter capacitor voltages and are denoted by v*sha, v*shb, and v*shc. The reference filter capacitors currents are computed using these reference voltages and are given as follows:

$$\begin{bmatrix} i_{sha}^* \\ i_{shb}^* \\ i_{shc}^* \end{bmatrix} = \omega C_{sh} e^{j90} \begin{bmatrix} v_{sha}^* \\ v_{shb}^* \\ v_{shc}^* \end{bmatrix}.$$

Unlike the predictive controllers, the hysteresis controller has the advantage of peak-current-limiting capacity apart from in addition to other merits such as extremely good dynamic performance, simplicity in implementation, and independence from load parameter variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with it. The switching signals generated for the VSI are as follows:

$$u_c = -K(z - z_{\text{ref}})$$

$$u = \text{hys}(-K(z - z_{\text{ref}})).$$ --24

If h ≥ lim then hys (h) = −1, bottom switch is turned ON, whereas top switch is turned OFF (Sa = 0,
S'a = 1).

If h ≤ lim then hys (h) = 1, top switch is turned ON, whereas bottom switch is turned OFF (Sa = 1, S'a
= 0).

The control circuitry is simple for both topologies because only three switching commands are to be generated. These three signals along with the complementary signals will control all the switches of the inverter.

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5.   SIMULATION RSULTS

In order to validate the proposed topology simulation is carried out using MATLAB. The source currents and the terminal voltages are not balanced before compensation, but after compensation both are balanced and sinusoidal output is obtain. Using PI controller the voltages across the two capacitors are maintained constant to the reference value. The dc-link capacitors across the top and bottom are shown below.

The problems which affect the power quality in distribution systems are pertaining to the specifications of the loads. Some of the most popular effects are: the harmonics generated by nonlinear loads and unbalanced loads and the low-power factor of the loads. A part from nonlinear loads, events like motor starting, capacitor switching and unusual faults could also impose power quality (PQ) problems. Fixed, mechanical switched reactor/capacitor banks and Static VAR Compensator (SVC) have been employed in power industry for improvement of system performances.

These types of compensation have some disadvantages such as limited bandwidth, slower response, more losses and big size. Recently, due to fast extension of high power switching elements such as IGBTs and IGCTs, DSTATCOM is a shunt custom power devices, has been recognized the second generation compensator for power factor correction load.
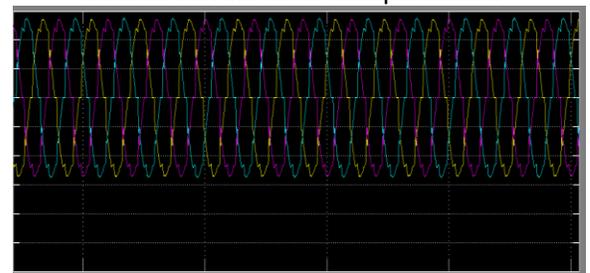
6.   CONCLUSION

A new hybrid topology is proposed in this paper, which has the capability of compensating the load at a lower dc-link voltage under non-stiff source. Design of the filter parameters is explained in detail. The proposed method is validated through simulation in a three phase distribution system. The proposed topology has less average switching frequency, less thresholds in the source currents and terminal voltages
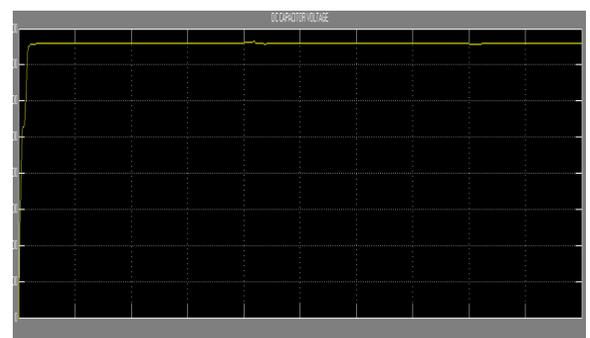
compared to the conventional topology.
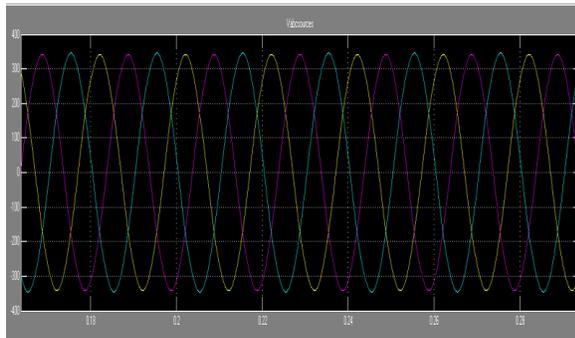
Simulation Results:
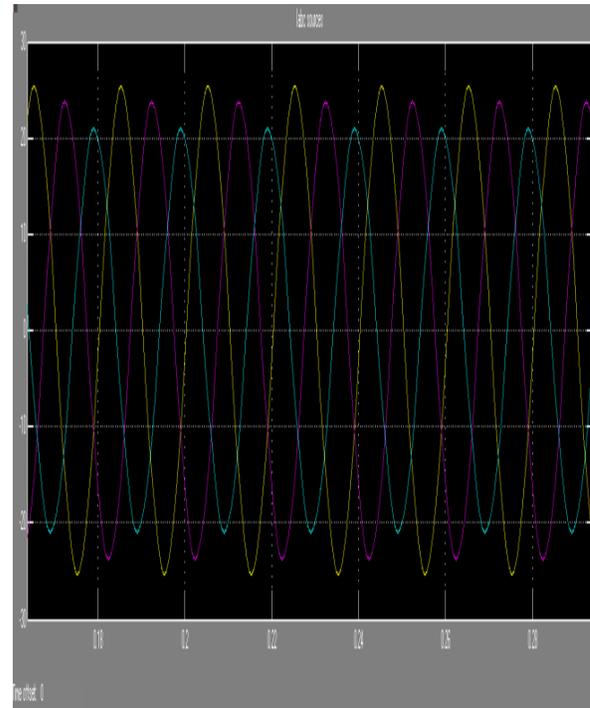
Source current after compensation

Filter current after compensation

Filter current after compensation

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Terminal voltage after compensation

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