1 BIT FULL ADDER CELL FOR REDUCING LOW LEAKAGE CURRENT IN NANO METER TECHNOLOGY

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Keywords:
Low leakage power;
Noise Margin;
Ground bounce noise;
Sleep transistor and Adder cell.

Abstract: *As technology scales into the nanometer regime ground bounce noise and noise immunity are becoming important metric of comparable importance to leakage current, active power, delay and area for the analysis and design of complex arithmetic logic circuits. In this paper, low leakage 1bit full adder cells are proposed for mobile applications with low ground bounce noise and a novel technique has been introduced with improved staggered phase damping technique for further reduction in the peak of ground bounce noise. Noise immunity has been carefully considered since the significant threshold current of the low threshold voltage transition becomes more susceptible to noise. We introduced a new transistor resizing approach for 1bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power and ground bounce noise. The simulation results depicts that the propose design also leads to efficient 1bit full adder cells in terms of standby leakage power, active power, ground bounce noise and noise margin. We have performed simulations using Cadence Spectra 90nm standard CMOS technology at room temperature with supply voltage of 1V.*

1. INTRODUCTION

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in Arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives.

The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life.

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For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call). When an electronic device such as a mobile phone is in standby mode, certain portions of the circuitry within the electronic device, which are active when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them, even though they have been de-activated. Even if the leakage current is much smaller than the normal operating current of the circuit. The leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. This is why building low leakage adder cells for mobile applications are of great interest. To summarize, some performance criteria are considered in the design and evaluation of adder cells, such as leakage

power, active power, ground bounce noise, area, noise margin and robustness with respect to voltage and transistor scaling as well as varying process and compatibility with surrounding circuitries.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30xincrease in gate leakage. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power.

Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further peak of ground bounce noise is possible with proposed novel technique with improved staggered phase damping technique.

This paper focuses on reducing sub threshold leakage power consumption and ground bounce noise.

The remainder of this paper is organized as follows. In section II, proposed nano-CMOS full adder circuits, and its equivalent circuits are discussed. In section III, the performance analysis and simulation results of conventional CMOS full adder cell and proposed circuitsare explained.

II. PROPOSED FULL ADDER CIRCUITS

Recently, power dissipation has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power dissipation.

Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous when we implement by the pass transistor logic. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability.

Fig. 1 shows the conventional CMOS 28 transistor adder. This is considered as a Base case throughout this paper. All comparisons are done with Base case.

The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs. Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a key role in static CMOS style. It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio does not give best results with respect to noise margin and standby leakage power when it is simulated in 90nm process. Modified adder circuits with sizing are proposed in Design1 and Design2 targeting the noise margin, and ground bounce noise.

Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with a proposed novel technique.

Modified sizing's are shown in Fig. 2 and Fig. 5 respectively. The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and gives W/L ratio of 1.2. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which is

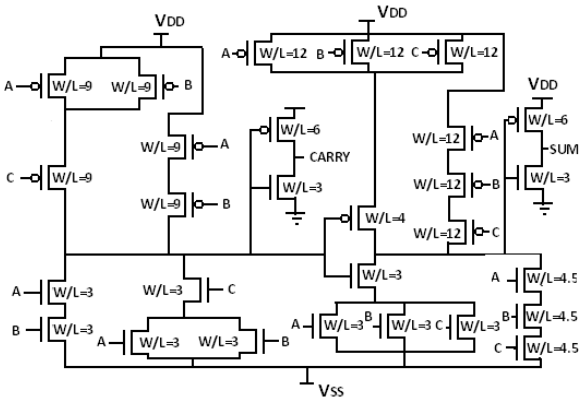


Figure 1. Conventional CMOS full adder.

3.1 times that of NMOS in Design1. The sizing of each block is based on the following assumption.

Base case is considered as individual block as shown in Fig. 3. Each block has been treated as an equivalent inverter. The same inverter ratio is maintained on each block. These sizing will reduce the standby leakage current greatly because subthreshold current is directly propotional to the Width/Length ratio of transistor. On the other hand, these reduced sizes will reduce the area occupied by the circuit. This will reduce the silicon chip area and obviously there will be a reduction in the cost.

Modified adder circuit i.e Design2 shown in Fig. 5, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an equivalent inverter. The same inverter size has been maintained on each block as shown in the Fig. 4. The goal of this design is to reduce the standby leakage power. Further compared to the Base case and Design1 and ground bounce noise produced when a circuit is connected to sleep transistor. However, there will be a slight variation on the noise margin levels and is almost equal to the Base case.

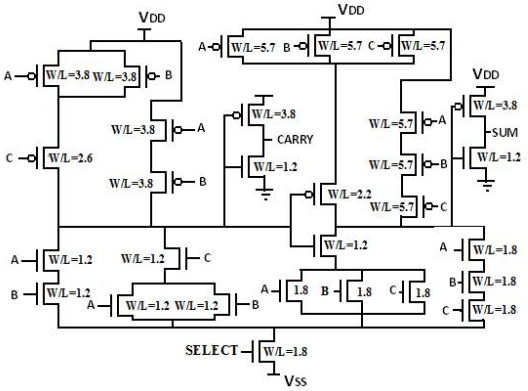


Figure 2. Proposed full adder (Design1) circuit with sleep transistor

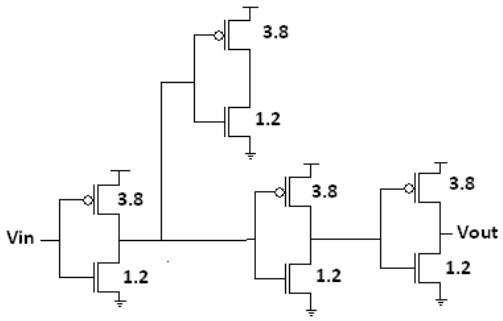


Figure 3. Equivalent circuit for Design1

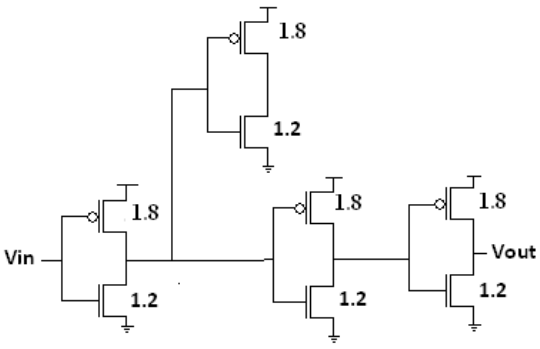


Figure 4. Equivalent circuit for Design2.

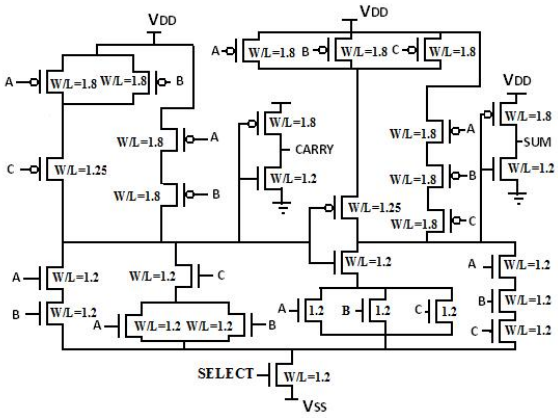


Figure 5. Proposed 1 bit full adder (Design2) circuit with sleep transistor

III. GATE-DIFFUSION INPUT

The basic GDI cell is shown in Fig. 5 while the truth table is shown in Table I. It should be noted that the source of the PMOS in a GDI cell is not connected to VDD while the source of the NMOS in a GDI cell is not connected to GND. This feature gives the GDI cell two extra input pins to use which makes the GDI design more flexible than an usual CMOS design. However, this feature is also the major cause of its disadvantage: special CMOS process required. To be more specific, the GDI scheme requires twin-well CMOS or silicon on insulator (SOI) process to implement which is of course more expensive than the standard p-well CMOS process

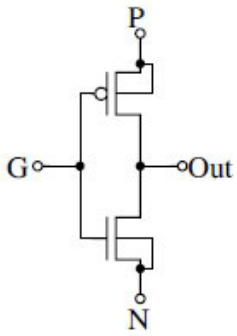
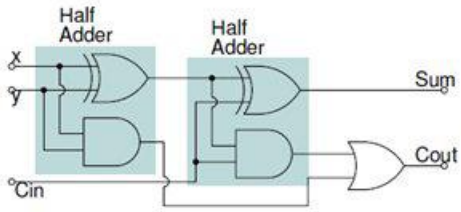
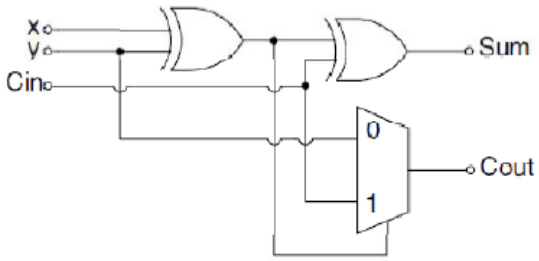


Fig. 6. Conventional CMOS full adder

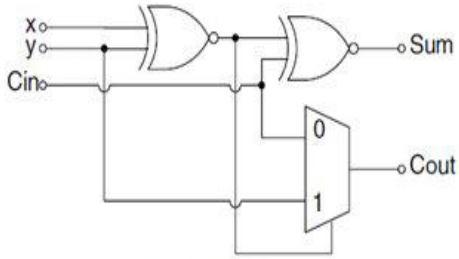


XOR/XNOR based full adder

According to equation (1) - (3), two XOR/XNOR based fulladders can be redesigned as shown in Fig. (a) and (b),respectively



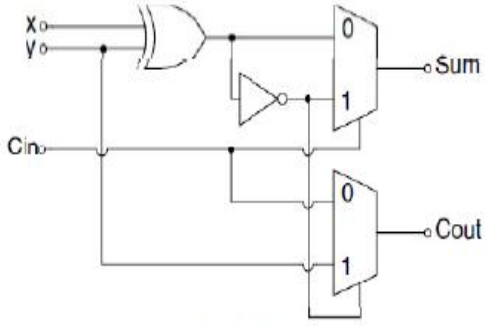
(a) XOR based full adder #1



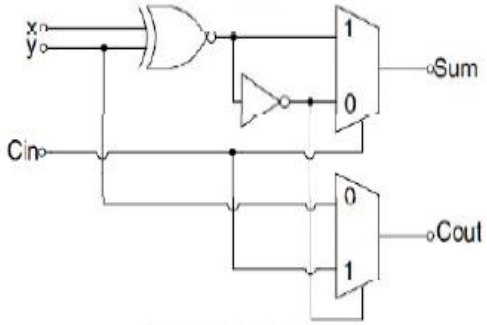
(b) XNOR based full adder #1

In addition, another two XOR/XNOR based full adders can be derived from equation (1), (2), and (4), respectively. The schematics are shown as Fig. 4(a) and 4(b) [7]. Compare Fig. 2 with Fig. 3 and Fig. 4, it is obvious that the architecture of the adders in Fig. 3 as well as Fig. 4 are simpler than that of Fig. 2. However, the conventional CMOS XOR, XNOR and MUX gates require too many transistors to build and thus are not preferred choices. In this case, the XOR, XNOR, and MUX gates are redesigned using GDI scheme.

The GDI XOR gate is shown as Fig. 5 where only 4 transistors are used. Compare the GDI XOR with the it's

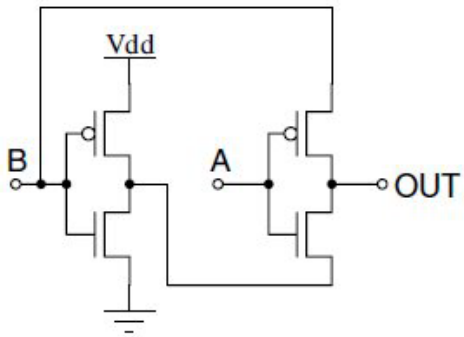


(a) XOR based full adder #2



(b) XNOR based full adder #2

Conventional CMOS counterpart, it is obvious that GDI XOR gate requires fewer transistors.



GDI XOR gate

B. GDI XNOR

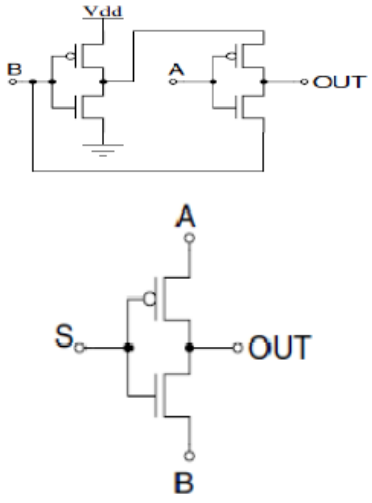
The GDI XNOR gate is shown as Fig. 6. It uses only 4 transistors as the GDI XOR gate does.

C. GDI MUX

Last but not least, a GDI MUX gate is implemented . The GDI MUX uses only 2 transistors.

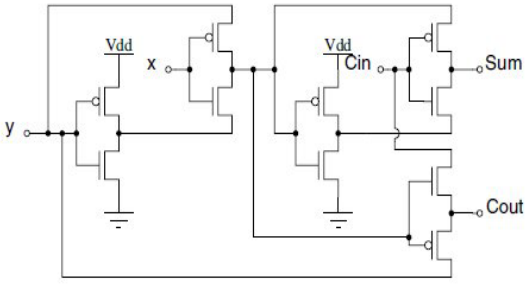
IV.THE PROPOSED GDI FULL ADDER

According to the mentioned 4 different full adder architectures, we can redesign 4 different types of GDI based full



GDI MUX gate

Adder. These 4 adders are shown. It should be noted that all of the proposed full adders are 10-T based. Hence, the attempt to create 10-T based full adders is achieved.



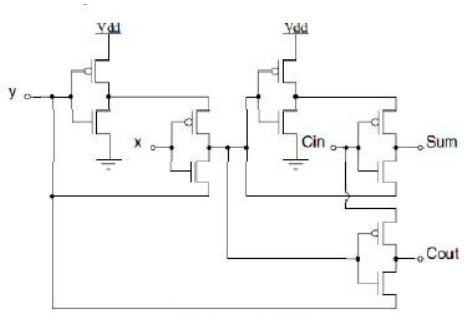
GDI XOR Full Adder #1

COMPARISON & IMPLEMENTATION

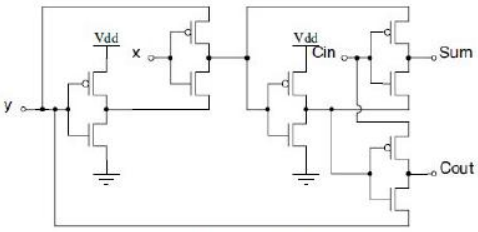
A. Comparison

In order to test the performance of the proposed GDI full adders, detailed comparisons are performed. The proposed designs are simulated using TSMC (Taiwan Semiconductor Manufacturing Company) 0.35μm 2P4M CMOS process. In addition, prior 10-T based full adder designs such as SEREF, YUKE9A, YUKE9B and YUKE13A are also included to compare with the proposed designs. In order to have a fair comparison, all the prior designs are recreated using the mentioned CMOS process. Besides, the transistor sizes of the prior designs are properly tuned to have optimal performance.

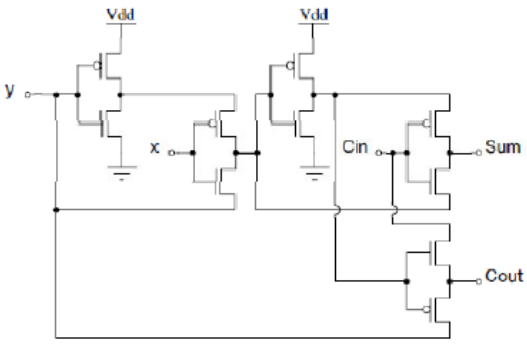
Although we have performed variety comparisons under different temperature circumstances like 0°C, 25°C,



GDI XNOR Full Adder



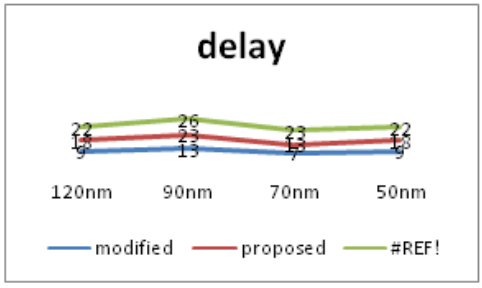
GDI XOR Full Adder

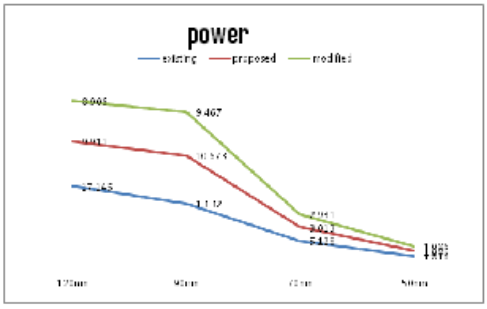


GDI XNOR Full Adder ‡

50°C, and 75°C, it is not likely to present all the comparison results due to page limitation. Thus, it should be noted that only comparison result at 25°C is presented as shown in Table II. Please also be noted that the bold faced numbers indicate the minimal value of each column. It is very obvious that the proposed GDI XNOR FA #2 has the minimal Power Delay product. Besides, the proposed GDI XOR FA #1 also Possesses very small Power Delay product. Hence, the proposed GDI XNOR FA #2 is the optimal 10-T based full adder design while the proposed GDI XOR FA #1 is also a preferable choice.

V.RESULTS





VI.CONCLUSION

In this paper, 4 refined GDI based 10-T full adders are proposed. The proposed designs possesses the advantages of flexibility, less transistor counts, and can be realized using standard p-well CMOS process. In addition, a chip using the proposed designs is implemented. The chip is realized by Micro wind 90 nm, 0.12um and 70 nm CMOS technology. The comparison between our designs and prior works indicates that one of our designs does provide its advantages. In short, the proposed designs can be taken a better alternative.

REFERENCES

1. Radu Zlatanovici, Sean Kao, Borivoje Nikolic, "Energy-Delay of Optimization 64-Bit Carry- Lookahead Adders With a 240ps 90nm CMOS Design Example," *IEEE J. Solid State circuits*, vol.44, no. 2, pp. 569-583, Feb. 2009.

2. K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhai, "Low-Power and High-Performance 1-bit CMOS Full Adder Cell," *Journal of Computers*, Academy Press, vol. 3, no. 2, Feb. 2008.

3. Rabaey J. M., A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, 2nd Prentice Hall, Englewood Cliffs, NJ, 2002

4. Pren R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid- State Circuits*, vol. 32, pp. 1079–1090, July 1997.

5. S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006.

6. K.Bernstein et al., "Design and CAD challenges in sub-90nm CMOS technologies," *in Proc.* int. conf. comput. Aided Des. 2003, pp.129-136.

7. "International Technology Roadmap for Semiconductors," Semiconductor Industry Association, 2005. [Online].

8. H.Felder and J.Ganger,"Full Chip Analysis of Leakage Power Under Process variations, Including Spatial Correlations, "in *proc. DAC*, pp.523-528, June 2005.

9. Jun Cheol Park and Vincent J. Mooney" Sleepy Stack Leakage Reduction" *IEEE* transactions on very large scale integration (vlsi) systems, vol.14, no.1. november 2006.

10. Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J. Nowka,"Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating,"*IEEE Transactions on VLSI Systems*,Vol.15, No.11, November2007.